

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output, comprising the steps of:

5 sampling an input voltage at a first clock rate onto an input sampling capacitor;
 dumping charge from the input sampling capacitor to the non-inverting input of the amplifier at
a second time and at the first clock rate;
 sampling a reference voltage onto a feedback sampling capacitor at substantially the first clock
rate;
10 dumping charge stored on the feedback sampling capacitor to the non-inverting input of the
amplifier at a second clock rate different than the first clock rate; and
 controlling the amount of time that charge is dumped from the feedback sampling capacitor to
be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor;
 wherein varying the second clock rate relative to the first clock rate changes the gain of delta-
15 sigma converter.

2. (Currently Amended) The method of Claim 1, wherein the steps of sampling an input voltage at the first clock rate onto an input sampling capacitor and dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprise:

5 generating a first clock with a first stream of periodic pulses at the first clock rate;
 generating a second clock with a second stream of periodic pulses and shifted in phase from
the first clock and synchronous therewith;
 sampling the input voltage onto the feedback sampling capacitor during the time that the first
stream of pulses are high; and

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10 dumping charge from the input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high.

3. (Original) The method of Claim 2, wherein the first stream of periodic pulses and the second stream of periodic pulses are non overlapping.

4. (Original) The method of Claim 2, wherein:

the step of sampling the input voltage on the input sampling capacitor comprises the steps of connecting one plate of the input sampling capacitor to the input voltage and the other plate of the input sampling capacitor to ground during the time that the first stream of pulses are high; and

5 the step of dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the input sampling capacitor to ground and the other plate of the input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high.

5. (Currently Amended) The method of Claim 2, wherein the steps of sampling the reference voltage onto the feedback sampling capacitor and dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier comprises the steps of:

5 sampling the reference voltage onto the feedback sampling capacitor during the time that the first stream of pulses are high; and

dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high and at a different clock rate than the step of sampling the reference voltage onto the feedback sampling capacitor.

6. (Currently Amended) The method of Claim 5, wherein:

the step of sampling the reference voltage on the feedback sampling capacitor comprises the steps of connecting one plate of the feedback sampling capacitor to the reference voltage and the other plate

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of the feedback sampling capacitor to ground during the time that the first stream of pulses are high; and
the step of dumping charge from the feedback sampling capacitor to the non-inverting input of
the amplifier comprises the steps of connecting the one plate of the feedback sampling capacitor to ground and
the other plate of the feedback sampling capacitor to the non-inverting input of the amplifier during the time that
the second stream of pulses are high and at a different clock rate than the step of sampling the reference voltage
onto a feedback sampling capacitor.

7. (Original) The method of Claim 6, wherein the step of dumping charge stored on the feedback
sampling capacitor to the non-inverting input of the amplifier occurs during the time that select ones of the pulses
in the second stream of pulses are high, and the number of the pulses in the second stream of pulses during
which the step of dumping charge stored on the feedback sampling capacitor to the non-inverting input of the
amplifier is less than all of the pulses in the second stream of pulses.

8. (Original) The method of Claim 7, and further comprising the step of generating a control signal
that selects the ones of the pulses in the second stream of pulses during which charge stored on the feedback
sampling capacitor is dumped to the non-inverting input of the amplifier.

9. (Currently Amended) Gain control circuitry for driving the input of an integrator in a delta-
sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a
reference voltage and an integration capacitor connected between the non-inverting input and the output,
comprising:

an input sampling circuit for sampling an input voltage at a first clock rate onto an input sampling
capacitor;

a first dump circuit for dumping charge from said input sampling capacitor to the non-inverting
input of the amplifier at a second time and at the first clock rate;

a feedback sampling circuit for sampling a reference voltage onto a feedback sampling
capacitor at substantially the first clock rate;

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a second dump circuit for dumping charge stored on said feedback sampling capacitor to the non-inverting input of the amplifier at a second clock rate different than the first clock rate; and

a gain control input for receiving a gain control input controller for controlling the amount of time that charge is dumped from said feedback sampling capacitor relative to be substantially equal to the amount of time that charge is being dumped from said input sampling capacitor;

wherein varying the second clock rate relative to the first clock rate changes the gain of delta-sigma converter.

10. (Currently Amended) The gain control circuitry of Claim 9, wherein said first sampling circuit and said first dump circuit comprise:

a first clock for generating a first stream of periodic pulses at the first clock rate;

a second clock for generating a second stream of periodic pulses and shifted in phase from said first clock and synchronous therewith;

first switching circuitry for sampling the input voltage onto the non-inverting input of the amplifier during the time that the first stream of pulses are high; and

second switching circuitry for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high.

11. (Original) The gain control circuitry of Claim 10, wherein said first stream of periodic pulses and said second stream of periodic pulses are non overlapping.

12. (Original) The gain control circuitry of Claim 10, wherein:

said first switching circuitry includes:

a first switch for connecting one plate of said input sampling capacitor to the input voltage, and

a second switch for connecting the other plate of said input sampling capacitor to ground during the time that the first stream of pulses are high; and

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said second switching circuitry includes:

a third switch for connecting the one plate of said input sampling capacitor to ground,

and

a fourth switch for connecting the other plate of said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high.

13. (Currently Amended) The gain control circuitry of Claim 10, wherein said second sampling circuit and said second dump circuit comprise:

third switching circuitry for sampling said reference voltage onto the non-inverting input of the amplifier during the time that the first stream of pulses are high; and

second switching circuitry for dumping charge from said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high and at a different clock rate than the clock rate at which the reference voltage is sampled onto said feedback sampling capacitor.

14. (Currently Amended) The gain control circuitry of Claim 13, wherein:

said third switching circuitry includes:

a fifth switch for connecting one plate of said feedback sampling capacitor to the reference voltage, and

a sixth switch for connecting the other plate of said feedback sampling capacitor to ground during the time that the first stream of pulses are high; and

said fourth switching circuitry includes:

a seventh switch for connecting the one plate of said feedback sampling capacitor to ground, and

a eighth switch for connecting the other plate of said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses are high and at a different clock rate than the clock rate at which the reference voltage is sampled onto said feedback sampling capacitor.

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15. (Original) The gain control circuitry of Claim 14, wherein dumping of charge stored on said feedback sampling capacitor to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses, and the number of the pulses in the second stream of pulses during which dumping of charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier is less than all of the pulses in the second stream of pulses.

16. (Original) The gain control circuitry of Claim 15, and further comprising a control signal that selects the ones of the pulses in the second stream of pulses during which charge stored on the feedback sampling capacitor is dumped to the non-inverting input of the amplifier.

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